WHAT IS CLAIMED:

1. An apparatus, comprising:

a provision for user input;

a provision for output;

a central processing unit (CPU) coupled to said user input and output;

a temperature level detector for detecting temperatures within said apparatus; and

a CPU sleep manager adapted to receive detected temperature levels from said temperature level detector, said CPU sleep manager selectively stopping clock signals from being sent to said central processing unit (CPU) when said detected temperature rises to a level at and above a selected reference temperature level.

2. The apparatus of Claim 1, wherein said user input is coupled to a keyboard.

3. The apparatus of Claim 1, wherein said output is coupled to a display device.

4. An apparatus, comprising:

a provision for user input;

a provision for output;

a central processing unit (CPU) coupled to said user input and output;

a CPU activity and temperature level detector, said temperature level detector detecting temperatures within said apparatus; and

a CPU sleep manager adapted to receive detected CPU activity and temperature levels from said CPU activity and temperature detector, said CPU sleep manager selectively stopping clock signals from being sent to said central processing unit (CPU) when said detected temperature rises to a level at and above a selected reference temperature level.

5. An apparatus, comprising:

a provision for user input;

a provision for output;

a central processing unit (CPU) coupled to said user input and output;

a CPU activity and temperature level detector, said temperature level detector detecting temperatures within said apparatus; and

a CPU sleep manager adapted to receive detected CPU activity and temperature levels from said CPU activity and temperature level detector, said CPU sleep manager selectively stopping clock signals from being sent to said central processing unit (CPU) when said detected temperature rises to a level at and above a selected reference temperature level and said CPU is processing non-critical I/O.

6. An apparatus, comprising:

a provision for user input;

a provision for output;

a central processing unit (CPU) coupled to said user input and output, said central processing unit (CPU) receiving one of a first clock signal at a first speed or a second clock signal at a second speed; and

a CPU sleep manager adapted to receive temperature levels detected within said apparatus and further adapted to designate that said central processing unit (CPU) receives said first clock signal when said detected temperature is at a level below a selected reference temperature level and receives said second clock signal when said detected temperature is at a level at and above said selected reference temperature level.

7. An apparatus, comprising:

a provision for user input;

a provision for output;

a central processing unit (CPU) coupled to said user input and output, said central processing unit (CPU) receiving one of a first clock signal at a first speed or a second clock signal at a second speed; and

a CPU sleep manager adapted to receive detected CPU activity and temperature levels associated with CPU operation and further adapted to designate that said central processing unit

(CPU) receives said first clock signal when said detected temperature is at a level below a selected reference temperature level and receives said second clock signal when said detected temperature is at a level at and above said selected reference temperature level.

8. An apparatus, comprising:

a provision for user input;

a provision for output;

a central processing unit (CPU) coupled to said user input and output, said central processing unit (CPU) receiving one of a first clock signal at a first speed or a second clock signal at a second speed; and

a CPU sleep manager adapted to receive detected CPU activity and apparatus temperature levels and further adapted to designate that said central processing unit (CPU) receives said first clock signal when said detected temperature is at a level below a selected reference temperature level and receives said second clock signal when said detected temperature is at a level at and above said selected reference temperature level and said CPU is processing non-critical I/O.

9. An apparatus, comprising:

a provision for user input;

a provision for output;

a central processing unit (CPU) coupled to said user input and output;

a temperature level detector for detecting temperatures within said apparatus; and

a CPU sleep manager adapted to receive detected temperature levels from said temperature level detector, said CPU sleep manager reducing central processing unit (CPU) clock speed when said detected temperature level is at and above a selected reference temperature level.

10. An apparatus, comprising:

a provision for user input;

a provision for output;

a central processing unit (CPU) coupled to said user input and output;

a CPU activity and temperature level detector, said temperature level detector detecting

temperatures within said apparatus; and

a CPU sleep manager adapted to receive detected CPU activity and temperature levels from said CPU activity detector, said CPU sleep manager reducing central processing unit (CPU) clock speed when said detected temperature level is at and above said selected reference temperature level.

11. An apparatus, comprising:

a provision for user input;

a provision for output;

a central processing unit (CPU) coupled to said user input and output;

a CPU activity and temperature detector, said temperature level detector detecting temperatures within said apparatus; and

a CPU sleep manager adapted to receive detected CPU activity and temperature levels from said CPU activity and temperature detector, said CPU sleep manager reducing central processing unit (CPU) clock speed when said detected temperature level is at and above said selected reference temperature level and said CPU is processing non-critical I/O.

12. A device, comprising:

a central processing unit (CPU); and

means for determining whether said central processing unit (CPU) may rest based upon a temperature level within said device and activating a hardware selector based upon said determination.

13. A device, comprising:

a central processing unit (CPU); and

means for determining whether said central processing unit (CPU) may rest based upon a temperature level within said device and activating a hardware selector based upon said determination.

14. The device of Claim 13, wherein the hardware selector applies oscillations to the clock input of said central processing unit (CPU) at a slower sleep clock level if the central processing unit is to sleep or rest or at a higher full processing rate speed clock level if the central processing unit is to be active.

15. The device of Claim 13, wherein the hardware selector prevents the oscillations from reaching the clock input of said central processing unit (CPU) if the central processing unit is to sleep or rest or supplies oscillations at the full processing rate speed clock level if the central processing unit is to be active.

16. The device of Claim 13, wherein said central processing unit (CPU) is part of a ~~computer.~~

17. A computer, comprising:

means for predicting temperature levels relevant to the operation of a central processing unit within said computer; and

means for using said prediction for automatic temperature control, said temperature control remaining transparent to a user of said computer.

18. A computer, comprising:

means for predicting activity and temperature levels within said computer; and

means for using said prediction for automatic temperature control, said temperature control remaining transparent to a user of said computer.

19. The computer of Claim 17, including means for user modification of said automatic temperature level predictions and using said modified predictions for automatic temperature control.

20. The computer of Claim 18, including means for user modification of said automatic activity and temperature level predictions and using said modified predictions for automatic temperature control.

21. An apparatus, comprising:

a central processing unit (CPU);

means for sampling a temperature level within said apparatus; and

means for automatically adjusting the processing speed of said central processing unit (CPU) to maintain said temperature level within said apparatus below a selected reference temperature level.

22. An apparatus, comprising:

a central processing unit (CPU);

means for sampling the activity and temperature levels of said central processing unit (CPU); and

means for automatically adjusting the processing speed of said central processing unit (CPU) to maintain said temperature level of said central processing unit (CPU) below a selected reference temperature level.

23. The apparatus of Claim 21, wherein said adjustments are accomplished within the central processing unit (CPU) cycles and do not affect the user's perception of performance.

24. A device, comprising:

a central processing unit (CPU) coupled to a clock;

means for sampling a temperature level within said device; and

means, responsive to said sampled temperature level, for controlling periods of time said clock is in an OFF state, the length of said periods of time said clock is in an OFF state being appropriate to allow said central processing unit to operate at a temperature level below a selected reference temperature level.

25. The device of Claim 24, wherein energy consumption in said device is at a maximum when the length of each period of time said clock is in an OFF state is at zero.

26. The device of Claim 24, wherein energy consumption in said device decreases as the length of each period of time said clock is in an OFF state increases.

27. The device of Claim 24, wherein said periods of time said clock is in an OFF state are constantly being adjusted to allow said central processing unit to operate at a temperature level below a selected reference temperature level.

28. The device of Claim 24, wherein said OFF state represents the minimum clock rate at which said central processing unit can operate.

29. The device of Claim 28, wherein said minimum clock rate may be zero for central processing units that can have their clocks stopped.

30. The apparatus of Claim 1 wherein said CPU sleep manager further sleeps a PCI bus coupled to the central processing unit (CPU).

31. The apparatus of Claim 30 wherein said CPU sleep manager further sleeps any other CPUs connected to the PCI bus.